# Curriculum Vitae

**DR. RAVNEET KAUR**

C1-102 Gold Croft C.G.H.S
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ravneetsawhney13@gmail.com

## Academic Background

| S.No. | Exam Passed | Year of passing | Name of the institution | Max Marks | Marks Obtained | % Marks |
|---|---|---|---|---|---|---|
| 1. | Xth (CBSE ) | 1997 | Lady Irwin Senior Secondary School, Canning Lane, New Delhi | 500 | 414 | 82.80 |
| 2. | XIIth (CBSE ) | 1999 | Lady Irwin Senior Secondary School, Canning Lane, New Delhi | 500 | 404 | 80.80 |
| 3. | B.S.c.(H) Electronics | 2002 | Atma Ram Sanatan Dharma College, Delhi University | 1500 | 1271 | 84.75 |
| 4 | M.Sc. Electronics | 2004 | Department of Electronic Science, University of Delhi South Campus | 1400 | 1124 | 80.23 |
| 5 | PhD Electronic Science | 2008 | Department of Electronic Science, University of Delhi South Campus | - | - | - |

**Thesis Title**: - *Analytical Analysis, Characterization and Simulation of Sub-100nm Advanced MOSFET Designs for improved Hot Carrier Reliability and RF/ Analog Performance*

- Qualified U.G.C ***NET (Lectureship),*** **June 2004 Exam**
- Qualified ***GATE*** 2004 Exam with **90.18 percentile**

## Teaching Experience and Courses Taught

***POST GRADUATE LEVEL***

| Course | Designation | Duration |
|---|---|---|
| M.Sc Electronics (1st Semester)- High Level Computer Language (C++)-1.1 *(Department of Electronic Science, University of Delhi South Campus)* | Guest Lecturer | 29 July 2004–21 November 2004 |
| | | 25 July 2005–22 November 2005 |
| | | 24 July 2006–24 November 2006 |
| | | 23 July 2007–23 November 2007 |
| | | 20 July 2008–13 November 2008 |

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|---|---|---|
| M.Sc Electronics (1st Semester)-High Level Computer Language and Operating System (lab course)-1.5<br>***(****Department of Electronic Science, University of Delhi South Campus****)*** | Guest Lecturer | 25 July 2005–22 November 2005<br>24 July 2006–24 November 2006<br>23 July 2007–23 November 2007<br>20 July 2008–13 November 2008 |
| ***UNDER GRADUATE LEVEL*** | | |
| **Annual Mode**<br>B. Sc.(H) Electronics II year -Numerical Analysis and FORTRAN Programming-2.7<br>B. Sc.(H) Electronics III year -Communication Lab-3.8<br>*(Deen Dayal Upadhyaya College, University of Delhi)* | Guest Lecturer | 19 July 2005 – 8 March 2006 |
| **Annual Mode**<br>**B.Sc.(H) Electronics: Part-III**<br>Communications (Paper 3.3)<br>Material Science and Integrated Circuit (Paper 3.5)<br>Electrical Technology and Electrical Machines (Paper 3.6)<br>Engineering Drawing (Paper 3.2)<br>Electronics Practical-III (Paper 3.8)<br>Electronics Practical and Projects (Paper 3.9)<br>**B.Sc.(H) Electronics: Part-II**<br>Instrumentation (Paper 2.4)<br>Numerical Analysis (Paper 2.7)<br>Electronics Practical-II (Paper 2.9)<br>**B.Sc.(H) Electronics: Part-I**<br>Electronics Practical-I (Paper 1.9)<br>**B.Sc. (Programme) APS, PS, ALS, LS: Part-I**<br>Electronics Laboratory-I (Paper PS 102.2)<br>**Semester Mode**<br>**B.Sc.(H) Electronics: Semester VI**<br>Digital Communication (ELHT 602)<br>Electronics Practical-XI (ELHP 605)<br>**B.Sc.(H) Electronics: Semester IV**<br>Numerical Techniques (Paper ELHT 401)<br>Electronics Practical-VII (ELHP 405)<br>Electronics Practical-VIII (ELHP 406)<br>**B.Sc.(H) Electronics: Semester III**<br>Electronics Practical-V (ELHP 305)<br>Electronics Practical-VI (ELHP 306)<br>**B.Sc.(H) Electronics: Semester I** | Ad-hoc Lecturer<br><br>Assistant Professor | 21 November 2007-19 March 2009<br><br>20 March 2009- Till Date |

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| Engineering Materials (ELHT 102)<br><br>**B.Sc.(H) Computer Science: Semester-II**<br>Hardware lab based on Digital Electronics (CS 207)<br>Digital Electronics (paper 104) ***(Old Course)***<br><br>**B.Sc.(H) Computer Science: Semester-I**<br>Digital Electronics (ELHT 301)<br>Lab based on Digital Electronics (ELHP 301)<br><br>***Four Year Undergraduate Program (FYUP)***<br><br>**B.Tech (Electronics) : Semester I**<br>Foundation Course –Information Technology (FC3IT)<br><br>**B.Tech (Electronics): Semester II**<br>Lab based on EL-DC-I-501(Signal and System)<br><br>**B.Tech (Electronics): Semester III**<br>Lab based on EL-DC-1-301 (Analog Electronics)<br>Lab based on EL-DC-1-302 (Digital system Design)<br><br>**B.Tech (Electronics): Semester IV**<br>EL-DC-I -402 (Electronic Instrumentation)<br>Lab based on EL-DC-I -402 (Electronic Instrumentation)<br><br>***Choice Based Credit System (CBCS)***<br>**B.Sc.(H) Electronics: Semester III**<br>Lab based on Digital Electronics and VHDL<br>Lab based on C Programming and Data Structures<br>C Programming and Data Structures.<br><br>**B.Sc.(H) Electronics: Semester IV**<br>Lab based on Signals and Systems<br><br>**B.Sc.(H) Electronics: Semester V**<br>Lab based on Numerical Analysis<br><br>**B.Sc.(H) Electronics: Semester VI**<br>Communication Electronics | | |

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| Lab based on Communication Electronics<br>Lab based on Electrical Machines<br>*(Acharya Narendra Dev College,* ***University of Delhi)***<br><br>***Choice Based Credit System (CBCS) with Learning Outcomes based Curriculum Framework (LOCF)***<br>**B.Sc.(H) Electronics: Semester III**<br>Lab based on C Programming and Data Structures<br>C Programming and Data Structures.<br><br>**B.Sc.(H) Electronics: Semester VI**<br>Communication Electronics<br>Lab based on Communication Electronics<br>*(Acharya Narendra Dev College,* ***University of Delhi)***<br>***Under Graduate Curriculum Framework -2022***<br>**B.Sc.(H) Electronics: Semester I**<br>Programming Fundamentals using Python- ELSDC-1 | | |

# Research Interest

**Modeling and simulation of sub-100 nm MOSFET structures:**

- **Channel Engineered**
- **Insulated Shallow Extension (ISE)**
- **Silicon on Insulator (SOI)**
- **Silicon on Nothing (SON)**
- **Grooved/ Concave Gate**

## Brief Overview of Research Work done till date

My research areas include analytical analysis, characterization and simulation of short channel effects in sub-100nm MOSFET for high performance. The work involves the physics based analytical modeling of MOS devices and simulating their intrinsic and terminal characteristics using numerical simulation software - ATLAS 2D and ATLAS 3D. The two-dimensional simulation and analytical modeling of sub-100nm gate-engineered Insulated Shallow Extension (ISE) devices and Grooved/ Concave Gate MOSFET for high performance RF and microwave applications has been done. My present research areas focus on the development of efficient 2D algorithms and optimization techniques for advanced sub-100nm MOS devices. Consideration has also been given to exploration of new architectures of Silicon on Insulator and Silicon On Nothing MOSFETs for enhanced performance and their applications in various different fields. I have also started with modeling and simulations of HEMTs for high performance microwave circuits.

My initial work in 2007 was based on the development of a new simple and computationally efficient two-dimensional analytical model for various advanced channel engineered MOSFET structures such as Epi-layer, Graded channel (GC), Lightly doped drain (LDD), Halo, Pocket implant technology etc for channel lengths down to 90 nm gate length, incorporating the effect of DIBL. The subthreshold drain

current model using Voltage Doping Transformation (VDT) method, replaced the influence of the lateral drain-source field by an equivalent reduction in the channel doping concentration.

In later part of 2007, a non-conventional MOSFET architecture of Insulated Shallow Extension (ISE) was studied. Substantial theoretical contributions had been made by developing compact models for Sub- 90 nm, ISE MOSFET for mixed mode applications. Electrical characteristics of 50nm DMG-ISE Gate stack MOSFET were investigated by extensive simulation studies using the non-local transport mechanisms of velocity overshoot and carrier diffusion due to electronic temperature gradients. By incorporating DMG architecture hot carrier reliability was improved and projects better linearity performance along with improvement in device intrinsic gain, voltage gain and $I_{on}/I_{off}$ ratio. Further, for improving the short channel behaviour of an ISE MOSFET, the use of gate stack consisting of a thin interfacial oxide layer and High k layer has also been envisaged.

## Research Experience

- ***Junior Research Fellow (JRF)*** in DRDO sponsored project entitled, "***Two Dimensional Physics Based Modeling and Simulation of a Graded Channel (GC) Multiple Gate SOI- MOSFET for sub 100nm Device Dimension for High Performance Analog Application*****".**

  **(1 April 2005 – 30 April 2007)**
- ***Senior Research Fellow (SRF)*** in DRDO sponsored project entitled, "***Two Dimensional Physics Based Modeling and Simulation of a Graded Channel (GC) Multiple Gate SOI- MOSFET for sub 100nm Device Dimension for High Performance Analog Application*****,"**

  **(1 May 2007 - 20 November 2007)**

## Administrative Experience

***Year 2022-2024***
Member, Purchase Committee, Department of Electronics
Member, NSS
Member-Stock Verification Committee
Member-Finance Committee
Member - Women Students Affairs Committee "SASHAKT"
Member-Internal Quality Assurance Cell (IQAC) of the college
Department Coordinator-Committee for DBT Star College Scheme

***Year 2020-2022***
Member, Admission Committee
Member, NSS
Member, ECA Committee for admissions
Member-Internal Quality Assurance Cell (IQAC) of the college
Member – Women Students Affairs Committee "SASHAKT"
Department Coordinator-Committee for DBT Star College Scheme

***Year 2019-2020***
Member, Admission Committee
Member, Purchase Committee, Department of Electronics
Member, Music Society -Dhun
Member, Library Committee

Department Coordinator-Committee for DBT Star College Scheme

***Year 2018-2019***
Teacher-in-Charge, Department of Electronics
Member, Admission Committee
Member, Purchase Committee, Department of Electronics
Member, Library Committee
Member, Time Table and Workload Committee
Member of the Faculty of Inter-disciplinary & Applied Sciences under the provision of Statute 9(3) (v) & 9(4)- Teacher's Category
Member-Internal Quality Assurance Cell (IQAC) of the college
Department Coordinator-Committee for DBT Star College Scheme

***Year 2017-2018***
Teacher-in-Charge, Department of Electronics
Member, Admission Committee
Member, Purchase Committee, Department of Electronics
Member, Library Committee
Member, Time Table and Workload Committee
Member-Alumni Affairs committee
Member-Academic Event management committee
Member of the Faculty of Inter-disciplinary & Applied Sciences under the provision of Statute 9(3) (v) & 9(4)- Teacher's Category
Member-Stock Verification Committee
Member-Internal Quality Assurance Cell (IQAC) of the college
Department Coordinator-Committee for DBT Star College Scheme

***Year 2016-2017***
Member-Alumni Affairs committee
Member-Academic Event management committee
Member of the Faculty of Inter-disciplinary & Applied Sciences under the provision of Statute 9(3) (v) & 9(4)- Teacher's Category
Member-AICTE approval committee- Committee for recognition for B.Tech in Computers and Electronic Courses
Department Coordinator-Committee for DBT Star College Scheme

***Year 2014 – 2016***
Member-IT Committee
Member- Remedial Coaching Committee
Member, Proctorial Committee
Member-Stock Verification Committee
Member-AICTE approval committee- Committee for recognition for B.Tech in Computers and Electronic Courses

***Year 2012 – 2014***
Teacher-in-Charge, Department of Electronics
Member, Admission Committee
Member, Purchase Committee, Department of Electronics
Member, Library Committee
Member, Time Table and Workload Committee
Member-IT Committee

Member- Finance Committee
Member-Stock Verification Committee

***Year 2011 – 2012***
Member- IT Committee
Member- Finance Committee
Member-Stock Verification Committee

***Year 2010 – 2011***
Member – Central Purchase Committee
Member – IT Committee
Member-Stock Verification Committee

***Year 2009 – 2010***
Member – Central Purchase Committee
Member – IT Committee
Member-Stock Verification Committee

***Year 2008 - 2009***
Member – IT Committee
Member – Central Purchase Committee
Member – Women Students Affairs Committee "SASHAKT"
Member- Electronics Club

***Year 2007 – 2008***
Member- Electronics Club

## Industry Experience

Centre for development of telematics **(CDOT**) at Pusa road, Summer Intern in ***Data communication in optical medium.***
Worked on C-DOT ***OMUX-32*** **(May2003-July2003)**

## Honours/Awards and Special Achievements

- Chaired a session in International Conference on Advances in IoT, Security with AI (ICAISA-2023) at Deen Dayal Upadhyaya College, University of Delhi, Sector-3, Dwarka, New during 24-25 March 2023.
- Received Award of Excellence for excellent mentorship towards paper presentation in "ICONICS-UG" held on 15th February 2021, Organised by Department of Electronics, Sri Aurobindo College, University of Delhi, India.
- Co-chaired a session in the international e-conference on 'Mitigating environmental issues by sustainable approaches (ICMCESA-2022)' organized by Acharya Narendra Dev College, University of Delhi from February 22-28, 2022, under the aegis of IQAC and DBT Star College Scheme.
- Expert Reviewer for IT related Vocational Education courses at **Bhartiya Shiksha Board (BSB)**
- Name listed in 2012 edition of ***Who's Who in the Academics***
- Name listed in 2009 edition of ***Who's Who in the World***
- ***Reviewer of*** **Journal of Electrical and Electronics Engineering Research (JEEER)**
- Name appeared in the ***Golden Report Selections T-ED***, IEEE Transactions on Electron Devices, vol. 55, no. 12, December 2008

- ***Reviewer of IEEE Transaction on Electron Devices***
- ***Reviewer of International Conference - Asia Pacific Microwave Conference (APMC)-2008*** *,16-19, December 2008 in Hong Kong Convention and Exhibition Center, Hong Kong, China*.
- ***Awarded full fellowship in Fourteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2007)*** Mumbai, December 16-20, 2007.
- Received ***All India Post Graduate Scholarships*** for the tenure of Post graduation, M.Sc (Electronics).
- ***Gold medallist*** in M.Sc.Electronics**,** University of Delhi South Campus and received ***Smt. Shanti Devi Bhargava Memorial Gold medal*** for being the best candidate in the M. Sc. Examination in Electronics in 2004.
- Got **2nd** position in B.Sc.(H) Electronics, University of Delhi..
- Awarded cash prize and Certificate of Merit for securing 1st position in college in B.Sc(H) Electronics for all the three years.

## Membership of Professional Societies

- American Nano Society- http://members.nanosociety.us/Ravneet
- Member IEEE, USA–Membership No. 90476328 - 9 years
  from 01 January, 2009 to 31 December, 2010.
  from 01 January, 2012 to 31 December, 2013.
  from 01 January, 2015 to 31 December, 2016.
  from 01 January, 2021 to 31 December, 2023.

- IEEE Electron Devices Society Membership - 7 Years
  from 01 January, 2012 to 31 December, 2013.
  from 01 January, 2015 to 31 December, 2016.
  from 01 January, 2021 to 31 December, 2023.

- IEEE Communications Society Membership- 1 Year
  from 01 January, 2010 to 31 December, 2010.

- IEEE Signal Processing Society Membership – 1 Year
  from 01 January, 2022 to 31 December, 2022.

- IEEE Young Professional Membership- 5 Years
  from 01 January, 2015 to 31 December, 2016.
  from 01 January, 2021 to 31 December, 2023.

## Computer Proficiency

- ***Operating systems*** **:** Familiar with ***MS-DOS***, ***WINDOWS, Linux.***
- ***Languages*** **: *C,C++, FORTRAN***, ***VHDL ,*** assembly language for ***8085, 8086*** Microprocessor
- ***Package*** **:** Knowledge of ***MS-Office***
- ***Digital Design Software*** **: *MAX+PLUS II***
- ***Circuit Design Software*** ***: Multisim, ORCAD and PSPICE***
- ***Simulators*** ***:BPM_CAD , ATLAS 2D , ATLAS 3D***
- ***Data Acquisition Software: LabVIEW***
- Knowledge of ***MATHCAD*** and familiarity with **SQL**

## Linguistic Proficiency

Hindi, English and Punjabi

## Personal Details

**Father's Name** S. Inder Dev Singh
**Date of birth** 13/12/1981
**Nationality** Indian
**Marital status** Married

## Projects undertaken

- Served as a mentor for ELITE- Education in a Lively Innovative Training Environment Scholarship programme by the college

| S.No. | Year | Project Title | Mentors |
|---|---|---|---|
| 1. | 2012 | Physics Based Numerical Problem-Solving Using Mathcad. | Dr. Ravneet Kaur<br>Dr. Sona P. Kumar |

- Served as a mentor for thefollowing DBT Star and DBT Star Elite Projects under DBT Star College Scheme 2017- 2020.

| **DBT STAR PROJECTS (2017-2020)** | | |
|---|---|---|
| **S.NO.** | **PROJECT TITLE** | **MENTORS** |
| | **2017-2018** | |
| | **DBT STAR Project** | |
| 1. | Plant electro stimulation and data acquisition | Dr. Ravneet Kaur (Electronics)<br>Dr. Udaibir Singh (Electronics)<br>Dr. Anita Narang (Botany)<br>Ms. Gauri Ghai (Electronics) |
| 2. | Assistive Gadgets for Visually Impaired Students<br>a) Light to Sound Convertor/ Optocoupler<br>b) Color Detector | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |
| 3. | Mine Detection Drone | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |
| | **DBT STAR ELITE Project** | |
| 4. | Lab Maintenance Application | Dr Ravneet Kaur<br>Ms Gauri Ghai |
| 5. | Communication Tool Kit by LabVIEW | Dr Ravneet Kaur<br>Dr Anita Kumari |
| | **2018-2019** | |
| | **DBT STAR Project** | |
| 6. | Smart Dustbin (Sensobin) | Dr. Ravneet Kaur<br>Dr. Monika Bhattacharya |
| | **DBT STAR ELITE Project** | |
| 7. | Security Device Development using Face Recognition Techniques "SWAN" | Dr Ravneet Kaur<br>Dr Monika Bhattacharya |

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| 8. | PUSTAK-Android Application Development | Dr Ravneet Kaur<br>Dr Monika Bhattacharya |
| 9. | Digital Laboratory Thermometer | Dr Ravneet Kaur<br>Ms. Gauri Ghai |
| 10. | B.A.T (Blind Assistance Toolkit) | Dr Ravneet Kaur<br>Dr Anita Kumari |
| 11. | Laser Security and Music System | Dr Ravneet Kaur<br>Ms. Gauri Ghai |
| 12. | **Text to Speech Converter** | Dr Ravneet Kaur<br>Ms. Gauri Ghai |
| | **2019-2020** | |
| | **DBT STAR Project** | |
| 13. | **Magnetic Collision Anti-Collision System** | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |
| 14. | **Solar Piezoelectric Charger (Piezoelectric Energy Harvesting System)** | Dr. Ravneet Kaur<br>Dr. Monika Bhattacharya |
| 15. | Gesture Recognizing Smart System | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |
| 16. | Automatic Titrator | Dr. Ravneet Kaur<br>Dr. Monika Bhattacharya |
| 17. | Wifi-Controlled Robot | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |
| | **DBT STAR ELITE Project** | |
| 18. | **Data Transfer through CPU Fans** | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |
| 19. | **Electrostimulation in plants** | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |
| 20. | Blind Assistance Toolkit (B.A.T) | Dr. Ravneet Kaur<br>Dr. Monika Bhattacharya<br>Ms. Gauri Ghai |
| 21. | Door Access Control Based on Face Recognition | Dr. Ravneet Kaur,<br>Dr. Monika Bhattacharya<br>Ms. Gauri Ghai |
| 22. | Laser Security & Music System | Dr. Ravneet Kaur |
| | **2020-2021** | |
| | **DBT STAR Project** | |
| 23. | Gesture Recognizing Smart System using Flex Sensors | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |
| 24. | Virtual Lab for Electronics: To design a 3-dimensional virtual laboratory to carry out experiments of circuit theory and semiconductor devices lab. | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |
| | **2021-2022** | |
| | **DBT STAR Project** | |
| 25. | Designing of a First Order Low-pass and High-pass filter using op-amp (Virtual Lab Development) | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |
| 26. | Study of the I-V Characteristics of the Common Base Configuration of BJT and obtain ri, ro, α. (Virtual Lab Development) | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |

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| 27. | To build a Flip- Flop Circuits using elementary gates. (JK Master Slave) (Virtual Lab Development) | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |
| 28. | To determine the value of Boltzmann Constant by studying forward-bias characteristics of a diode. (Virtual Lab Development) | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |
| 29. | To verify Malus Law (Virtual Lab Development) | Dr. Ravneet Kaur<br>Ms. Gauri Ghai |

- Served as Mentor for the project "**Sensors based Notification System for Visually Impaired Persons**" funded by National Science and Technology Entrepreneurship Development Board (NSTEDB) of the Department of Science &Technology of one-year duration ,2013-2014 and total amount: Rs 82,000/-.

- "8085 Microprocessor based ***Traffic Light Controller with a Digital Counter***".

  ***Description*-In this, the 8085 microprocessor was interfaced with a seven segment digital displays and LEDs to provide provisions for regulating traffic flow. The programming using 8085 assembly language is done including interrupts for pedestrians.**

- "Validation and study of ***Data communication in optical medium***" using Optical multiplexing unit OMUX-32.

  ***Description-D*ata communication in optical medium was studied and its practical implementation on the CDOT Optical Multiplexing Unit, OMUX-32 was done. The specification of the said unit was verified using power spectrum analyzer.**

- Worked on "***Design and simulation of Integrated Optical Devices*** using BPM CAD".

  ***Description*-In this, *d*esign, simulation and optimization of proton-exchange integrated optical devices such as linear waveguide, power splitters, power combiners, directional couplers and electro optic switch using BPM CAD tool was performed. The effect of annealing these optical devices was studied and their output power integrals were obtained for optimization purpose.**

## Workshops / Seminars/ Conferences Attended

1. Resource Person in a five-day workshop on "Development of Audio Video Resources based on Laboratory Manual in Science at Upper Primary Stage" held at DESM, NCERT, New Delhi from February 27, 2022 to March 03, 2022.
2. Attended Virtual Mini Colloquia (MQ) on "75th Anniversary of Transistor Invention" organised by IEEE EDS Delhi Chapter (New Delhi, India) from August 22, 2022 to August 29, 2022.
3. Attended IPR awareness/training program under the special mission called "National Intellectual Property Awareness Mission (NIPAM)" organised by Acharya Narendra Dev College, University of Delhi on August 27, 2022.
4. Attended One Week Online Workshop on "Recent Development in the Field of Electronics (RDFE-2022)" organised by Department of Electronic Science, University of Delhi, in collaboration with IEEE EDS and IEEE APS & CRFID Delhi Chapter from July 25, 2022 to July 29, 2022.
5. Resource Person in National Workshop on Skill Enhancement of Non-Teaching Staff (NWSENS-2022) organised by Acharya Narendra Dev College from July 13 to July 20, 2022.

6. Attended 6-Day Bootcamp entitled “Virtual Lab Development 1.0” organized by ANDC, University of Delhi, New Delhi from January 17, 2022 to January 22, 2022.
7. Attended the webinar on, “Understanding Plagiarism Detection Software Ouriginal” organized by University of Delhi in Association With eGalactic Pune on January 28, 2022.
8. Attended the Training Program on “New Measurement Technologies and Simulation Techniques in Electronics" organized by IEEE Electron Device Society-Delhi Chapter & Department of Electronic Science, University of Delhi South Campus during October 17-18, 2022.
9. Attended Special Mini Colloquia (MQ) in Virtual Mode on "Emerging Device Architectures for Tunnel FET" as part of the "75th Anniversary of Transistor Invention" organized by IEEE Electron Device Society - Delhi Chapter (New Delhi, India), The National Academy of Sciences India - Delhi Chapter and Deen Dayal Upadhyaya College (University of Delhi) during September 26 to October 5, 2022.
10. Participated and successfully completed National Online FDPs- 106 Big Data organised by University of Delhi in collaboration with GAD-TLC, a Centre under PMMMNMTT, Ministry of Education, Government of India held from 04 to 11 November 2022.
11. Resource Person in a five-day workshop on “Development of Competency Framework and Revisiting of the Learning Outcomes in Science and Mathematics (PAC 6.01/2021-22)” held online at DESM, NCERT, New Delhi from March 7, 2022 to March 11, 2022.
12. Resource Person in a five-day workshop on “Development of Competency Framework and Revisiting of the Learning Outcomes in Science and Mathematics (PAC 6.01/2021-22)” held online at DESM, NCERT, New Delhi from February 28, 2022 to March 4, 2022.
13. Resource person in a five-day workshop on “Online Course in Teaching of Science at Upper Primary Stage.” held online at DESM, NCERT, New Delhi from January 10, 2022 to January 14, 2022.
14. Resource person in a five-day workshop on “Online Course in Teaching of Science at Upper Primary Stage.” held online at DESM, NCERT, New Delhi from January 17, 2022 to January 21, 2022.
15. Resource Person in one-day interaction programme “Science Adda”, held on December 20, 2021, organized under the DBT Star College Scheme by Acharya Narendra Dev College.
16. Delivered a lecture as a “Resource Person” on the topic Communication: Past, Present and Future on February 3, 2022, organized by Internal Quality Assurance Cell (IQAC) of ARSD College.
17. Attended 6-Day Bootcamp entitled “Virtual Lab Development 1.0” organized by ANDC, University of Delhi, New Delhi from January 17, 2022 to January 22, 2022.
18. Attended the webinar on, “Understanding Plagiarism Detection Software Ouriginal” organized by University of Delhi in Association With eGalactic Pune on January 28, 2022.
19. Resource Person in National Workshop on Skill Enhancement of Non-Teaching Staff (NWSENS-2022) organised by Acharya Narendra Dev College from July 13 to July 20, 2022.
20. Attended the Training Program on “New Measurement Technologies and Simulation Techniques in Electronics" organized by IEEE Electron Device Society-Delhi Chapter & Department of Electronic Science, University of Delhi South Campus during October 17-18, 2022.
21. Attended Special Mini Colloquia (MQ) in Virtual Mode on "Emerging Device Architectures for Tunnel FET" as part of the "75th Anniversary of Transistor Invention" organized by IEEE Electron Device Society - Delhi Chapter (New Delhi, India), The National Academy of Sciences India - Delhi Chapter and Deen Dayal Upadhyaya College (University of Delhi) during September 26 to October 5, 2022.
22. Attended a five-day workshop on ""“Online Course in Teaching of Science at Upper Primary Stage.” held online at DESM, NCERT, New Delhi from February 08, 2021 to February 12, 2021.
23. Attended Online Lecture Series on “Fundamentals and Applications of Technology Driven Sensors.” organised by IEEE EDS Delhi Chapter from September 24, 2021 to September 25, 2021.
24. Attended Vice-Chancellors' Conclave On "National Education Policy 2020: Its Implementation, Opportunities and Challenges" organized by Rajdhani College, University of Delhi, July 16, 2021.
25. Attended IP Awareness/Training program under National Intellectual Property Awareness Mission

organized by Intellectual Property Office, India on December 29,2021.

26. Participated in Online National workshop entitled" Tools and Techniques in Statistical Analysis" organized by Acharya Narendra Dev College, University of Delhi, New Delhi from April 6, 2021 to April 19, 2021.
27. Participated in Robonetics: 30 days intense workshop on "Robotics and it's analogy implementation" Organised by Tech Analogy from September 24, 2021 to October 23, 2021.
28. Attended International Symposium on "History and Future of Transistors" organised by IEEE EDS Delhi Chapter on December 23, 2021.
29. Attended a four-day workshop on ""Online Course in Teaching of Science at Upper Primary Stage." held online at DESM, NCERT, New Delhi from December 01, 2020 to December 04, 2020.
30. Attended the three-day workshop on "Development of Tactile Kit in Science at Upper Primary stage", organized by Department of Education in Science and Mathematics, NIE Campus, NCERT New Delhi from March 11, 2020 to March 13, 2020.
31. Attended the three-day workshop on "Development of Tactile Kit in Science at Upper Primary stage", organized by Department of Education in Science and Mathematics, NIE Campus, NCERT New Delhi from March 16, 2020 to March 20, 2020.
32. Attended a series of five Cyber Security Awareness webinars organized by Automation & Digitization Committee, Bhaskaracharya College of Applied Sciences, University of Delhi on June 23, July 3, July 14, July 29 and August 29, 2020.
33. Attended International webinar series "Technological Trends for the Next Generation" organized by Department of Electronics, Bhaskaracharya College of Applied Sciences, University of Delhi from June 1-5, 2020.
34. Attended a five-Day Online Workshop on MOODLE: Learning Management System organized by Department of Electronics and Department of English, Shaheed Rajguru College of Applied Sciences for Women, University of Delhi from June 8-12, 2020.
35. Attended one Day Faculty Development Programme on "Machine Learning" on 4th March 2020 at Acharya Narendra Dev College, University of Delhi (DU), New Delhi.
36. Attended the IEEE Electron Devices Society DL Mini Colloquium (Virtual) on Mini Colloquium on "Emerging Nano Devices and Circuits – The Roadmap Ahead" organized by Department of Electronic Science, University of Delhi South Campus and IEEE Electron Devices Society Delhi Chapter – India from October 5-9, 2020.
37. Attended National One Week Online Faculty Training Program on "PEDAGOGICAL TRAINING FOR EFFECTIVE ONLINE TEACHING & LEARNING" organized by Deen Dayal Upadhyaya College (University of Delhi) and K.T.H.M. College, Nashik, Maharashtra under the Internal Quality Assurance Cell (IQAC) & DBT Star College Program from August 3-10, 2020.
38. Attended online Summer School cum Faculty Development Program on Advances in Signal Processing and Machine Learning organized by MHRD-Institution Innovation Council, DDUC Chapter, Deen Dayal Upadhyaya College, University of Delhi (under the aegis of Science Foundation and DBT Star College Program); Department of Electronic Science, University of Delhi; The National Academy of Sciences India (NASI)-Delhi Chapter and supported by IEEE Electron Device Society (EDS)-Delhi Chapter from July 20-26, 2020.
39. Attended four-day workshop on "Online Course in Teaching of Science at Upper Primary Stage." organized by Department of Education in Science and Mathematics, NIE Campus, NCERT New Delhi from December 1, 2020 to December 4, 2020.
40. Participated in the webinar on the topic "Medicinal Plants: Eternal Source of Health and Wellness", organized by the Department of Botany, Swami Shraddhanand College, University of Delhi, on June 17, 2020.
41. Attended the webinar, "A Short History of Solar Physics" organised by Department of Physics and Department of Instrumentation under the aegis of IQAC, Bhaskaracharya College of Applied Sciences held on July 30, 2020 through Google Meet
42. Participated in the One Day National Webinar entitled "ICT Enabled Higher Education in India"

jointly organized by Guru Angad Dev Teaching Learning Centre, SGTB Khalsa College, University of Delhi under the Pandit Madan Mohan Malaviya National Mission on Teachers and Teaching (PMMMNMTT) of MHRD and Sanatan Dharma College, Ambala Cantt (Affiliated to Kurukshetra University, Kurukshetra) held on 13 July 2020. (This is equivalent to a regular National Seminar).

43. Attended National webinar on Enhancing "Research Interest" on research publication organised by IQAC, Maharaja Agrasen College on June 03, 2020.
44. Attended Global Bio-India Summit held in India in Aerocity, New Delhi from November 21-23, 2019. Department of Biotechnology (DBT), Ministry of Science & Technology, Government of India and Public Sector Undertaking, Biotechnology Industry Research Assistance Council (BIRAC) organized Global Bio-India Summit 2019, a mega international congregation of biotechnology stakeholders, including international bodies, regulatory bodies, Central and State Ministries, SMEs, large industries, bio-clusters, research institutes, investors, and the start-up ecosystem.
45. Attended a five-day workshop entitled 'Empowering Teachers: Current Technology Based Educational Content Creation' using open source and free software at Acharya Narendra Dev College, University of Delhi from December 2-6, 2019 under IQAC.
46. Resource Person in a three-day workshop for reviewing the Augmented Reality content developed for School Education. organized by CIET, NIE Campus, NCERT New Delhi from November 27-29, 2019. Attended the workshop on 28th November, 2019.
47. Invited Talk on "Use of ICT tools in teaching and learning Physics" in 7th Annual Convention of the Regional Council (Delhi & Haryana) of the Indian Association of Physics Teachers (IAPT) on 17th August, 2019 at N.C. Jindal Public School, Punjabi Bagh, New Delhi-110026.
48. Presented the paper "Gesture Controlled Robot: ELECTROMON" in Regional Competition on Innovative Experiments in Physics (RCIEP) 2019 on 17th August, 2019 during the Annual Convention of the Regional Council (Delhi & Haryana) of the Indian Association of Physics Teachers (IAPT)at Delhi at N.C. Jindal Public School, Punjabi Bagh, New Delhi - 110026.
49. Resource Person in a five-day workshop on "Implementation of intervention strategies and its effectiveness in the Achievement of learning outcomes in science at upper primary Stage. (PAC-6.02)" ", organized by Department of Education in Science and Mathematics, NIE Campus, NCERT New Delhi from 15th July- 19th July, 2019.
50. Resource Person in a five-day workshop on "Development of Audio-Video Resource on Experiments of Chemistry at Higher Secondary Stage (Class XI)" organized by Department of Education in Science and Mathematics, NIE Campus, NCERT New Delhi from February 25, 2019 to March 1, 2019. Attended the workshop from February 27, 2019 to March 1, 2019
51. Subject Expert in a five-day workshop on "Development of Tactile Kit in Science at Upper Primary stage", organized by Department of Education in Science and Mathematics, NIE Campus, NCERT New Delhi from February 11, 2019 to February 15, 2019.
52. Presented a Seminar Paper in the 06th three-week Refresher Course in Basic Science (Interdisciplinary) from September 26, 2018 to October 17, 2018, at UGC-HRDC, Jamia Millia Islamia, New Delhi.
53. Resource Person in a five-day workshop on "Development of Tactile Kit in Science at Upper Primary stage", organized by Department of Education in Science and Mathematics, NIE Campus, NCERT New Delhi from September 10, 2018 to September 14, 2018.
54. Resource Person in a five-day workshop on "A Study of Utilization of Science Laboratories in Learning Science in Higher Secondary Schools of NCR" organized by Department of Education in Science and Mathematics, NIE Campus, NCERT New Delhi from July 30, 2018 to August 03, 2018.
55. Resource Person in a five-day workshop on "Development of Tactile Kit in Science at Upper Primary stage", organized by Department of Education in Science and Mathematics, NIE Campus, NCERT New Delhi from March 19, 2018 to March 23, 2018.
56. Resource Person in a five-day workshop on "Development of Tactile Kit in Science at Upper Primary stage", organized by Department of Education in Science and Mathematics, NIE Campus, NCERT New Delhi from March 03, 2018 to March 16, 2018.

57. Resource Person in a five-day workshop on "Online Course in Teaching of Science at Upper Primary stage", organized by Department of Education in Science and Mathematics, NIE Campus, NCERT New Delhi from February 19, 2018 to February 23, 2018.
58. Resource Person in a five-day workshop on "Development of Tactile Kit in Science at Upper Primary stage", conducted at DESM, NCERT, NIE Campus, New Delhi from November 6, 2017 to November 10, 2017.
59. Participated in the Jury Process of INSPIRE (INNOVATION IN SCIENEC PURSUIT FOR INSPIRED RESEARCH) 4th National Level Exhibition and Project Competition organised by the Department of Science and Technology during October 06-08, 2014 at Pragati Maidan. New Delhi.
60. Participated in two day workshop on Use of Technologies in Teaching at Centre for Professional Development in Higher Education, University of Delhi, October 17-18, 2014.
61. Participated in two day workshop on Line Follower Robotics, held in collaboration with EFY group; Publishers of Electronics For You magazine at Bhaskaracharya College of Applied Sciences, University of Delhi, 11-12 March 2014.
62. Participated in the Jury Process of INSPIRE (INNOVATION IN SCIENEC PURSUIT FOR INSPIRED RESEARCH AWARD National Level Exhibition and Project Competition (NLEPC)-2013 organised by the Department of Science and Technology during October 08-10, 2013 at Pragati Maidan. New Delhi.
63. Attended "MATLAB & SIMULINK Academic Tour 2013" of Math works at Cluster Innovation Centre on September 23, 2013, University of Delhi.
64. Participated in the "National Workshop on VLSI Designing using Verilog Coding" organized by Bhaskracharya College of Applied Science, University of Delhi, 16-18 July 2013.
65. Participated in the workshop of Foundation Course- Information Technology at Centre for Professional Development in Higher Education, University of Delhi during May 23- 25, 2013.
66. Attended workshop on " Trans-disciplinary Areas of Research & Teaching by Shanti Swaroop Bhatnagar awardee at Deen dayal Updhyaya College, University of Delhi jointly organized by IEEE EDS Delhi Chapter, during February 01-02, 2013.
67. Participated in the Jury Process of ***INSPIRE (INNOVATION IN SCIENEC PURSUIT FOR INSPIRED RESEARCH AWARD National Level Exhibition and Project Competition (NLEPC)-2012*** organised by the Department of Science and Technology during October 21-23, 2012 at Pragati Maidan. New Delhi.
68. Attended Two Days ***Joint Science Academies Lecture Workshop On "History, Aspects and Prospects of Electronics in India"*** during October 12-13, 2012 at *:* SP Jain Centre Auditorium, University of Delhi South Campus, Benito Juarez Road, Dhaula Kuan, New Delhi, 110021
69. Attended Two Days Mini-Colloquia on "***Compact Modelling Techniques for Nanoscale Devices and Circuit Analysis***" during March 14-15, 2012 at Arts Faculty Building, University of Delhi South Campus, Benito Juarez Road, New Delhi, 110021
70. Participated in the workshop "***Experiments & Research Applications with National Instruments LabVIEW***" organized by Bhaskaracharya College of Applied Science (University of Delhi) Sec-2, Phase-I, Dwarka, New Delhi, 2-3 February 2012.
71. Attended National Seminar on ***Teaching Redefined: Open Access to Education***, organized by Acharya Narendra Dev College, University of Delhi, November 1, 2011.
72. Presented a paper entitled "Analytical Drain Current Evaluation Technique for Various Non-Uniformly Doped MOS Device Architectures" authored by Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta and also member of organizing committee in ***12th International Symposium on Microwave and Optical Technology (ISMOT-2009)*** organized by Department of Electronic Science, University of Delhi South Campus, Hotel Ashok, New Delhi, India, 16-19 December, 2009.
73. Attended Workshop on "***Easy Now-1:A Workshop on Multimedia Content Development***", jointly organized by Acharya Narendra Dev College, University of Delhi and Commonwealth Educational Media Centre for Asia during 20-25th April 2009.
74. Participated as Resource Person in the Workshop on "***Data Acquisition using LabVIEW and Printed***

***Circuit Board (PCB)- Designing and Fabrication***" organized by Department of Electronics, Acharya Narendra Dev College, University of Delhi during 10-20th June 2008.

75. Presented paper entitled "Impact of Gate Stack Configuration onto the RF/analog Performance of ISE MOSFET" authored by Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta in ***International Conference on Recent Advancements in Microwave Theory and Applications (Microwave-2008)***, Jaipur, India, November 21-24, 2008
76. Presented paper entitled "Simulation of a Novel ISE MOSFET with Gate Stack Configuration" authored by Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta in Second National Conference on ***Mathematical Techniques Emerging Paradigm for Electronics and IT Industries (MATEIT 2008)***, September 26-28, 2008 in New Delhi, India.
77. Presented paper entitled "TCAD Performance Investigation of a Novel MOSFET Architecture of Dual Material Gate Insulated Shallow Extension Silicon On Nothing (DMG ISE SON) MOSFET for ULSI era" authored by Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta in ***Asia Pacific Microwave Conference (APMC)-2008,*** 16-19, December 2008 in Hong Kong Convention and Exhibition Center, Hong Kong, China
78. Presented paper entitled "Analytical Analysis of Sub-Threshold Performance of Sub-100nm Advanced MOSFET Structures-An Iterative Approach" authored by Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta and member of organizing committee ***Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed mode Applications-2008***, 5-6 January, 2008, University of Delhi South Campus, New Delhi, India.
79. Presented paper entitled "Dual Material Gate (DMG) SOI-MOSFET with Dielectric Pockets: Innovative Sub-50 nm design for improved switching performance" authored by Ravneet Kaur, Rishu Chaujar, Manoj Saxena, and R. S. Gupta, ***Indo-Australian Symposium on Multifunctional Nanomaterials, Nanostructures and Applications (MNNA 2007)***, December 19–21, 2007, New Delhi, India.
80. Presented paper entitled "Effect of transport property on the performance of insulated shallow extension gate stack (ISEGaS) MOSFET" authored by Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta in ***Indian microelectronics Society Conference 2007 Theme: Trends in VLSI and Embedded System***, Panjab Engineering College, Chandigarh, India, August 17-18, 2007.
81. Attended Workshop on "***Linux and Open System Software***", organized by Open $L_X$ Linux held at Acharya Narendra Dev College, University of Delhi during 6-7th December 2007.
82. Attended National Workshop on ***VLSI Design and Embedded System (NWVDES)*** held at Birla Institute of Technology and Science, Pilani- 24-26 February 2006.
83. Presented paper entitled "RF Performance Investigation of Gate Stacked Insulated Shallow Extension (ISE) MOSFET and Bulk: A Comparative Study" authored by Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta in ***National Conference on Mathematical Techniques Emerging Paradigm for Electronics and IT Industries (MATEIT 2006)***, 24-26 March 2006, New Delhi, India.
84. Presented paper entitled "Lateral Channel Engineered Structure- Insulated Shallow Extension (ISE) MOSFET: DC and RF Performance Investigation" authored by Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta in ***National Conference on Recent Advancement in Microwave Technique and Applications (Microwave-2006)***, 6-8 October 2006, Jaipur, India
85. Presented paper entitled "Investigating the role of Stacked Gate Oxide and Hetro-Material Gate on Electrical Characteristics of Insulated Shallow Extension (ISE) MOSFET" authored by Ravneet Kaur, Manoj Saxena and R. S. Gupta in ***Thirteenth International Workshop on Physics of Semiconductor Devices (IWPSD-2005)***, Vol. 2, pp 1163-1166, 13-17 December 2005,New Delhi India.

## Workshops / Seminars/ Conferences Organised

1. One Day offline Workshop on Arduino and Sensor Interfacing on January 01, 2023 under the student SPIE chapter, under the aegis of IQAC and DBT Star College Scheme, Acharya Narendra Dev College, University of Delhi.
2. Workshop on Hologram Recording and Reconstruction on February 04, 2023 under the student SPIE

chapter, under the aegis of IQAC and DBT Star College Scheme, Acharya Narendra Dev College, University of Delhi.

3. Coordinator of the International e-conference on 'Mitigating Contemporary Environmental Issues by Sustainable Approaches (ICMCESA-2022)' organized by Acharya Narendra Dev College from February 22-28, 2022 under the aegis of IQAC and DBT Star College Scheme.
4. An outreach program for school students, "ECOVILLE" was organized on February 27, 2022 as a part of the E- conference that invited submission of avant-garde research projects, video presentations, environmental quiz and paper presentations.
5. Workshop on Full Stack Web Development using MERN organized under the DBT Star College Scheme by Acharya Narendra Dev College from March 5-9 2022.
6. Workshop on Holography organized under the DBT Star College Scheme by Acharya Narendra Dev College on March 14, 2022
7. Hands-on Workshop on Arduino and Sensor Interfacing in technical collaboration with industry partner Touch Techno Pvt. Ltd. organized under the DBT Star College Scheme by Acharya Narendra Dev College on March 26, 2022.
8. Training workshop and demonstration of Control Lab with software and data acquisition and Universal Dev Board with FPGA and CPLD for Teachers in collaboration with industry partner M/s Silicom Electronics organized under the DBT Star College Scheme by Acharya Narendra Dev College held on April 25, 2022.
9. Training Workshop and demonstration of lab Equipment for Teaching and Non- Teaching Staff in collaboration with industry partner M/s Vijayanta Electronics organized under the DBT Star College Scheme by Acharya Narendra Dev College held on March 23, 2022.
10. One Week National Workshop on Career and Skill Enhancement for Non-teaching Staff under the DBT Star College Scheme by Acharya Narendra Dev College from September 15-21, 2022
11. Hands-on Workshop on Arduino and Sensor Interfacing in technical collaboration with industry partner Touch Techno Pvt. Ltd. under the DBT Star College Scheme by Acharya Narendra Dev College on September 10, 2022.
12. Education visit to Nehru Planetarium, New Delhi. under the DBT Star College Scheme by Acharya Narendra Dev College on September 24, 2022.
13. Education visit to PM Museum (Pradhanmantri Sangrahalaya), New Delhi, New Delhi. under the DBT Star College Scheme by Acharya Narendra Dev College on September 24, 2022.
14. Webinar on "Career Opportunities in Publishing" under the student SPIE chapter and DBT star College Scheme. Acharya Narendra Dev College, University of Delhi on February 4, 2022.
15. One-day interaction programme "Science Adda", held on December 20, 2021, organized under the DBT Star College Scheme by Acharya Narendra Dev College.
16. Invited Talk on Creative Thinking and Enterpreneurial Skills by Dr. Ravinder Kaur, Associate Professor, Deptt. Of Electronics, Deen Dayal Upadhaya College, Delhi University on June 23, 2021.
17. Invited Talk on Digital Transformation and it's impact on the future after Covid-19 delivered by Dr. Amita Kapoor, Associate Professor, Shaheed Rajguru College of Applied Sciences on July 7, 2021.
18. One-week Hands on workshop on Cloud Computing in technical collaboration with industry partner M/s Brain Mentors Pvt. Ltd. from September5-September11, 2021.
19. Science Education Outreach Program on Sensor Interfacing using Arduino and TinkerCAD simulation from October 18- October 30, 2021.
20. Online: Python Workshop: Data Science with Python under the student SPIE chapter and DBT star College Scheme. Acharya Narendra Dev College, University of Delhi from March3-7, 2021.
21. Online five days LabView Workshop: to provide basic training and hands-on exposure to Virtual Instrumentation and LabView under the student SPIE chapter and DBT star College Scheme. Acharya Narendra Dev College, University of Delhi from June 23-27, 2021.

22. Online: Flutter Workshop: Hybrid Mobile App development with Flutter programming under the student SPIE chapter and DBT star College Scheme. Acharya Narendra Dev College, University of Delhi from July 13-17, 2021.
23. One day excursion/educational trip to National Science Centre, Pragati Maidan, on the occasion of *'Vigyan Samagam'*, India's first-ever, global Mega-Science exhibition under the student SPIE chapter and DBT star College Scheme. Acharya Narendra Dev College, University of Delhi on February 22, 2020.
24. Online five days LabView Workshop: to provide basic training and hands-on exposure to Virtual Instrumentation and LabView under the student SPIE chapter and DBT star College Scheme. Acharya Narendra Dev College, University of Delhi from June 23-27, 2020.
25. Online: Flutter Workshop: Hybrid Mobile App development with Flutter programming under the student SPIE chapter and DBT star College Scheme. Acharya Narendra Dev College, University of Delhi from July 13-17, 2020.
26. PCB Design and Fabrication (demostration of PCB Prototyping Machine) in technical collaboration with Excel Technologies, Noida on August 23, 2020.
27. Organized One Day Interdisciplinary Exhibit Presentation "New Frontiers in Science" at Acharya Narendra Dev College, University of Delhi under the aegis of DBT Star College Scheme on October 22, 2019.
28. Invited talk on 'Satellite Communication' by Prof. Mridula Gupta, Department of Electronic Science, University of Delhi under DBT star College Scheme. Acharya Narendra Dev College, University of Delhi on January 31, 2019.
29. Invited talk on 'Professional Conduct with Positive Attitude' by Ms. Anju Kumari, motivational speaker, Life skills trainer, Founder, Crafting leaders under DBT star College Scheme. Acharya Narendra Dev College, University of Delhi on October 4, 2018.
30. Invited talk on 'Current Trends in Mobile Application Development' by Mr. Rohit Gambhir, Lead in Mobile Application Development, QA Infotech under DBT star College Scheme. Acharya Narendra Dev College, University of Delhi on September 20, 2018.
31. Invited talk on 'A Preface into Wireless Communication and Electronic Warfare' by Mr Sourabh Basu, Scientist/ Engineer 'SE', ISRO Satellite Centre, Bangalore & Joint Deputy Director, NTRO, New Delhi under DBT star College Scheme. Acharya Narendra Dev College, University of Delhi on January 29, 2018.
32. Organised a visit to Centre for e-Governance, Department of Electronics and IT, for students of Acharya Narendra Dev College on March 14, 2014
33. Visit to Gandhi Bhawan for students of B.Tech (Electronics) I Semester and B. Tech.(Comp. Sc.) I Semester on October 15, 2013.
34. Visit to Centre for e-Governance, Department of Electronics and IT, for students of Acharya Narendra Dev College during 1st, 3rd, 4th and 7th October, 2013.
35. Organized a Lecture on "Internet of things" for students by Mr. Himanshu Gandhi, Sr. Tech Lead, Aricent Technologies on October 31, 2013.
36. Member of organizing committee for organizing alumni meet of Department of Electronics on October 31, 2013.
37. Organised a visit to Golden Temple and Wagah Border, Amritsar from December6-7, 2013.
38. Member of organizing committee in the Workshop on "***Emerging Trends in Electronics***"

    ***Workshop 1: Optical Fiber Communication***

    ***Workshop 2: Embedded Systems and Robotics***

    ***Workshop 3: Data Acquisition and Signal Processing using LabVIEW***

    Organized by Department of Electronics, Acharya Narendra Dev College, University of Delhi during 1-12$^{th}$ June 2009.

39. Part of Infrastructure Team in ***Symposium on recent advances in Telecommunication Systems and Technologies (2004)*** at University of Delhi South Campus.
40. Member of organizing committee in ***Asia Pacific Microwave Conference 2004 (APMC '04)***, 15-18 December, 2004.
41. Part of Infrastructure Team in ***National Symposium on recent advances in microwaves and light waves (NSAML'03)*** University of Delhi South Campus, New Delhi, October 2003
42. Member of organizing committee in Short course on "***Spice Models for Advanced VLSI Circuit Simulation***" organized by Department of Electronic Science, University of Delhi South Campus, 11-12 December, 2005.

# Refresher/ Orientation Course and Faculty Development Programme

- Attended one Day Faculty Development Programme on "Machine Learning" on 4th March 2020 at Acharya Narendra Dev College, University of Delhi (DU), New Delhi.
- Attended two Day Faculty Development Programme on "Emotional Intelligence" conducted by ICT Academy on 1st April 2019 to 2nd April 2019 at Acharya Narendra Dev College, University of Delhi (DU), New Delhi.
- Participated in 06th three weeks Refresher Course in Basic Science (Interdisciplinary) from September 26, 2018 to October 17, 2018, at UGC-HRDC, Jamia Millia Islamia, New Delhi.
- Participated in one day Faculty Development Programme "Teacher's as Mentors" at Acharya Narendra Dev College, University of Delhi on October 25, 2018.
- Attended Faculty Development Programme on "Research Methodology" held during 16-12-2017 to 22-12-2017, Internal Quality Assurance Cell, Bhaskracharya College of Applied Sciences, University of Delhi.
- Attended Faculty Development Workshop on "Embedded Systems and Synthesis of Nano-Materials",Department of Physics And Electronics and Internal Quality Assurance Cell, Hansraj College, University Of Delhi, January 6-7, 2017.
- Participated in 3 weeks Refresher Course in "E-Learning and Digital Learning (ID)" from September 05, 2017 to September 25, 2017, at Centre for Professional Development in Higher Education, University of Delhi, Delhi.
- Attended one-week Faculty Development Programme on "Advances in Microelectronics and Plasma Diagnostics" (AMPD-2016) during 29-8-2016 to 02-9-2016, Department of Applied Physics, Delhi Technological University, Delhi.
- Participated in the four-week Orientation Course organized during November 08, 2011 to December 02, 2011 at Academic Staff College, Jawaharlal Nehru University, New Delhi..

# List of publications

## Total Publications: 80

### Papers Published in International Referred Journals: 23

| Name of the Journal | No. of Articles | Impact Factor |
|---|---|---|

| | *As an author/ Corresponding author* | *As a Co-author* | ***(*ISI Thomson Impact Factor: 2022)** |
|---|---|---|---|
| *IEEE Transaction on Electron Devices* | 3 | 1 | 3.221 |
| *Semiconductor Science and Technology* | 2 | 3 | 2.048 |
| *Microelectronic Engineering* | 1 | 1 | 2.662 |
| *Superlattices and Microstructures* | | 4 | 3.22 |
| *International Journal of Numerical Modeling: Electronic Networks, Devices and Fields* | | 1 | 1.436 |
| *Microwave and Optical Technology Letter* | 1 | 1 | 1.311 |
| *Journal of Semiconductor Technology and Science* | | 1 | 0.561 |
| *Advances in Computer Science and Information Technology (ACSIT)* | | 1 | - |
| *DU Journal of Undergraduate Research and Innovation* | 1 | | - |
| Journal of Intelligent & Fuzzy Systems | | 1 | 1.737 |
| Journal of Engineering Education and Transformations | 1 | | - |

**Papers Published in International Conference: 44**
**Papers Published in National Conference: 13**
**Others**: 5

***Year Wise Publications***
***International Journals:***

**2007**

1. "Performance Investigation of 50nm **I**nsulated **S**hallow **E**xtension **G**ate **S**tack (ISEGaS) MOSFET for Mixed Mode Applications*,"* Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta, **IEEE Transactions on Electron Devices**, Vol. 54, No.2, pp. 365-368, February 2007.
2. "Hot carrier reliability and analog performance investigation of DMG-ISEGaS MOSFET", Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta, **IEEE Transactions on Electron Devices** Vol. 54, No. 9, pp. 2556-2561, September 2007.
3. "Unified Subthreshold Model for Channel Engineered Sub-100nm Advanced MOSFET Structures", Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta**, IEEE Transactions on Electron Devices ,** Vol. 54, No. 9, pp. 2475-2486, September 2007.
4. "Two-Dimensional Analytical Model to Characterize Novel MOSFET Architecture: Insulated Shallow Extension (ISE) MOSFET", Ravneet Kaur, Rishu Chaujar, Manoj Saxena, and R. S. Gupta, **Semiconductor Science and Technology**, Vol. 22, pp. 952-962, 2007**.**
5. "Lateral Channel Engineered - Hetero Material Insulated Shallow Extension Gate Stack (HMISEGAS) MOSFET Structure: High Performance RF Solution for MOS Technology", Ravneet Kaur, Rishu Chaujar, Manoj Saxena, and R. S. Gupta, **Semiconductor Science and**

**Technology** Vol. 22, pp. 1097-1103, 2007**.**

**2008**

6. "Laterally amalgamated DUal Material GAte Concave (L-DUMGAC) MOSFET For ULSI", Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, **Micro Electronic Engineering**, Vol. 85, No. 3, pp. 566-576, March 2008.
7. "Two-Dimensional Analytical Sub-Threshold Model of Multi-Layered Gate Dielectric Recessed Channel (MLaG-RC) Nanoscale MOSFET", Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, **Semiconductor Science and Technology,** Vol. 23**,** No.4**,** 045006 (10pp), April 2008.
8. "Intermodulation Distortion and Linearity Performance Assessment of 50-nm gate length L-DUMGAC MOSFET for RFIC Design", Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, **Superlattices and Microstructures,** Vol. 44, No.2, pp 142-153, August 2008.
9. "Investigation of Multi-Layered-Gate Electrode Workfunction Engineered Recessed Channel (MLGEWE-RC) Sub-50nm MOSFET: A Novel Design", Rishu Chaujar**,** Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, ***International Journal of Numerical Modeling: Electronic Networks, Devices and Fields*** (*Accepted July 2008*).
10. "TCAD Assessment of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET and its Multi-Layered Gate Architecture: Part-I: Hot Carrier Reliability Evaluation", Rishu Chaujar**,** Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, ***IEEE Transactions on Electron Devices,*** Vol. 55, No. 10, pp. 2602-2613, October 2008 .
11. "On-State and RF Performance Investigation of Sub-50nm L-DUMGAC MOSFET Design for High-Speed Logic and Switching Applications", Rishu Chaujar**,** Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, ***Semiconductor Science and Technology,*** Vol. 23, No.9, 095009, September 2008 .
12. **"**Modeling and Analysis of fully strained and partially relaxed lattice mismatched AlGaN/GaN HEMT for High Temperature Applications", Parvesh Gangwani, Ravneet Kaur, Sujata Pandey, Subhasis Haldar, Mridula Gupta and R.S. Gupta, ***Superlattices and Microstructures***, Vol. 44, No.6, pp 781-793, December 2008.

**2009**

13. "Two-Dimensional Analytical Modeling of a Novel Gate-Stack ISE MOSFET", Ravneet Kaur, Rishu Chaujar**,** Manoj Saxena and R. S. Gupta, **Micro Electronic Engineering** , Vol. 86, Issue 10, pp 2005-2014, October 2009.
14. "Two-dimensional threshold voltage model and design considerations for gate electrode work function engineered recessed channel nanoscale MOSFET: I", Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, ***Semiconductor Science and Technology***, Vol.24, 10pp, 2009..
15. "TCAD assessment of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET and its multi-layered gate architecture, Part II: Analog and large signal performance evaluation", Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, ***Superlattices and Microstructures***, Volume 46, Issue 4, Pages 645-655, October 2009.
16. "T-gate Geometric (Solution for Submicrometer Gate Length) HEMT: Physical Analysis, Modeling and Implementation as Parasitic Elements and its usage as Dual Gate for Variable Gain Amplifiers", Ritesh Gupta, Servin Rathi, Ravneet Kaur, Mridula Gupta and Radhey S Gupta, ***Superlattices and Microstructures,*** Volume 45, Issue 3, Pages 105-116, March 2009.

**2010**

17. "Hot Carrier Reliability Monitoring of DMG ISE SON MOSFET for Improved Analog Performance", Ravneet Kaur, Rishu Chaujar, Manoj Saxena, and R. S. Gupta, ***Microwave and Optical Technology Letters***, Vol.52, No.3, pp. 770-775, 2010.
18. "Design Considerations and Impact of Technological Parametric Variations on RF/Microwave Performance of GEWE-RC MOSFET", Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, ***Microwave and Optical Technology Letters***, Vol.52, No.3, pp.652-657, 2010.
19. "Metal Insulator Gate Geometric HEMT: Novel Attributes and Design Consideration for High Speed Analog Applications", Ritesh Gupta, Ravneet Kaur, Sandeep Kr Aggarwal, Mridula Gupta and R. S. Gupta, Journal of Semiconductor Technology and Science, Vol.10, No.1, Pages 66-76, March 2010.

**2016**

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